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EXAMINER	
TU, CHRISTINE TRINH LE	
ART UNIT	**PAPER NUMBER**
2138	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/518,226	CHRISTENSEN, CARL
	Examiner	Art Unit
	Christine T. Tu	2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12/29/2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leitch (5,559,506) in view of Cantarella (4,417,339).

Claim 1:

Leitch discloses the invention substantially as claimed. Leitch teaches (figures 3 & 5, 8, 12-14) that a data symbol set (730) contains N x Q x R information symbols which include N tiers (740), each tier having R rows by Q columns of information symbols. Each tier is later expanded to (Q + S) x (R + T) by adding S parity symbols to each row and by adding T column parity symbols for each column. Leitch further shows that a communication system comprises a receiving device (206) having a control circuit (206) for performing row parity checking and column parity checking. The control circuit (206) comprises a decoder (950) having a row parity checker (910) for determine whether a parity check of selected data symbols passes or fails. The decoder (950) also has a column parity checker (930) and a symbol corrector (940). The column parity checker (930) determines whether a parity check of the selected data symbols passes or fails. The parity checking results are coupled from the row parity checker (910) and the column parity checker (930) to the symbol corrector (940). The symbol correct (940) evaluates a tier of data symbols to correct those which have ambiguous errors (figures 3 & 5, 8, 12-14, column 9 lines 28-44, column 5 lines 33-42, column 15 line 4-column 16 line 56).

Leitch does not teach the parity check for each of the N rows and the X columns for detecting bit-level errors. However, Cantarella teaches that syndrome bits (S_1, S_2, ...S_{k-1}) from the parity check subcircuits (10, 12, 14) , are decoded in a decoder (20) to produce an output a CVECTOR (C_0, C_1 ... C_{m-1}) which identifies the bit in error in information bits (i_0, i_1, ..., i_{m-1}). Cantarella also teaches that if there is an error, a unique subset of OVP (S_1, S_2, ... S_{k-1}) will be one to identify the bit in error (figure 1, column 4 lines 12-18, column 7 lines 19-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Leitch's row and column parity check results from the row and the column parity checkers (910 & 930) can later be used for detecting any bit in error (as taught by Cantarella). One having ordinary skill in the art would be motivated to realize so because bit(s) in error(s) have to be detected in order to Cantarella's symbol corrector (940) to correct those error(s) (as taught by Cantarella [column 15 lines 51-60]).

Leitch does not explicitly teach the identifying at least one bad byte for the data block using a byte level error detection process. However, Leitch teaches (figure 18) that within each tier (steps 1810, 1880, 1890), the (Q + S) symbols in each of the (R + T) rows are checked for parity errors (step 1820), the (R + T) symbols in each of the (Q + S) columns is checked for parity errors (1830). The symbol corrector (940) determines all possible error patterns which satisfy the row and column parity checking results and identifies which of the possible errors are non-ambiguous or ambiguous and

corrects such errors therefrom (steps 1840-1870) (column 18 line 59-column 19 line 26).

It would have been obvious to one skilled in the art at the time the invention was made to realize that such checking row and column parity errors for each tier would encompass for checking errors for each tier itself. One having ordinary skill in the art would be motivated to do so because Leitch teaches that each tier of the N tiers would expand to (Q + S) columns and (R + T) rows by encoding the tier (figure 5, column 9 lines 35-58).

Claim 2:

Leitch's communication system (figures 3, 12 & 13) comprises row and column parity encoders (425 & 426) and a decoder (950).

Leitch does not explicitly teach 8B/10B. Leitch teaches (Q +S) bits of data wherein Q equals 4 and S equals 2. It would have been obvious to one skilled in the art at the time the invention was made to realize Leitch's Q could equal to 8 and S could equal to 2. One having ordinary skill in the art would be motivated to do so because (a) Leitch teaches that other values of Q and S may be used (column 9 lines 45-47) and (b) such Leitch's other values are not excluded from the inclusion of the value 8 for Q and therefore (Q+S) = (8+2) = 10.

Claim 3:

Leitch does not explicit teach 32 rows of data block. Leitch teaches R rows of data wherein R equals 3. It would have been obvious to one skilled in the art at the time the invention was made to realize Leitch's R could equal to 32. One having ordinary skill in the art would be motivated to do so because (a) Leitch teaches that other values of R may be used, (column 9 lines 45-47) and (b) such Leitch's other values are not excluded from the inclusion of the value 32.

Claim 4:

Leitch's control circuit (206) comprises a decoder (950) having a row parity checker (910) for determine whether a parity check of selected data symbols passes or fails (figures 5, 8, 12-14 & 18, column 15 line 4-column 16 line 56, column 18 line 59-column 19 line 26).

Claims 5-6:

Leitch's decoder (950) also has a column parity checker (930) and a symbol corrector (940). The column parity checker (930) determines whether a parity check of the selected data symbols passes or fails. The parity checking results are coupled from the row parity checker (910) and the column parity checker (930) to the symbol corrector (940). The symbol correct (940) evaluates a tier of data symbols to correct those which have ambiguous errors (figures 5, 8, 12-14 & 18, column 15 line 4-column 16 line 56, column 18 line 59-column 19 line 26).

Claims 7-10:

Claims (7 & 8) and (9-10) are rejected for reasons similar to those set forth against claims (5 & 4) and (5-6), respectively.

Claim 11:

Leitch teaches that the parity checking results are coupled from the row parity checker (910) and the column parity checker (930) to the symbol corrector (940). The symbol corrector (940) identifies errors determined by the row parity checker (910) and column parity checker (930) as ambiguous errors or non-ambiguous errors. The symbol correct (940) evaluates a tier of data symbols to correct those which have ambiguous errors (figures 3 & 5, 8, 12-14, column 9 lines 28-44, column 5 lines 33-42, column 15 line 4-column 16 line 56).

Claims 12 & 13:

Leitch discloses the invention substantially as claimed. Leitch teaches (figures 3 & 5, 8, 12-14) that a data symbol set (730) contains N x Q x R information symbols which include N tiers (740), each tier having R rows by Q columns of information symbols. Each tier is later expanded to (Q + S) x (R + T) by adding S parity symbols to each row and by adding T column parity symbols for each column. Leitch further shows that a communication system comprises a receiving device (206) having a control circuit (206) for performing row parity checking and column parity checking. The control circuit (206) comprises a decoder (950) having a row parity checker (910) for determine

whether a parity check of selected data symbols passes or fails. The decoder (950) also has a column parity checker (930) and a symbol corrector (940). The column parity checker (930) determines whether a parity check of the selected data symbols passes or fails. The parity checking results are coupled from the row parity checker (910) and the column parity checker (930) to the symbol corrector (940). The symbol correct (940) evaluates a tier of data symbols to correct those which have ambiguous errors (figures 3 & 5, 8, 12-14, column 9 lines 28-44, column 5 lines 33-42, column 15 line 4-column 16 line 56).

Leitch does not explicitly teach the identifying at least one suspect bit in a data block. However, Leitch teaches (figure 18) that within each tier (steps 1810, 1880, 1890), the (Q + S) symbols in each of the (R + T) rows are checked for parity errors (step 1820), the (R + T) symbols in each of the (Q + S) columns is checked for parity errors (1830). The symbol corrector (940) determines all possible error patterns which satisfy the row and column parity checking results and identifies which of the possible errors are non-ambiguous or ambiguous and corrects such errors therefrom (steps 1840-1870) (column 18 line 59-column 19 line 26).

It would have been obvious to one skilled in the art at the time the invention was made to realize that such checking row and column parity errors for each tier would encompass for checking errors for each tier itself. One having ordinary skill in the art would be motivated to do so because Leitch teaches that each tier of the N tiers expand to (Q + S) columns and (R + T) rows by encoding the tier (figure 5, column 9 lines 35-58).

Leitch does not teach that the identifying steps is performed using information derived from a byte level error detect process and information derived from a bit-level error detection process. However, Cantarella teaches that syndrome bits (S_1, S_2, ...S_{k-1}) from the parity check subcircuits (10, 12, 14) , are decoded in a decoder (20) to produce an output a CVECTOR (C_0, C_1 ... C_{m-1}) which identifies the bit in error in information bits (i_0, i_1, ...; i_{m-1}). Cantarella also teaches that if there is an error, a unique subset of OVP (S_1, S_2, ... S_{k-1}) will be one to identify the bit in error (figure 1, column 4 lines 12-18, column 7 lines 19-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Leitch's row and column parity check results from the row and the column parity checkers (910 & 930) can later be used for detecting any bit in error (as taught by Cantarella). One having ordinary skill in the art would be motivated to realize so because bit(s) in error(s) have to be detected in order to Cantarella's symbol corrector (940) to correct those error(s) (as taught by Cantarella [column 15 lines 51-60]).

<u>Claims 14 and 15:</u>

Leitch's communication system (figures 3, 5, 12 & 13) comprises row and column parity encoders (425 & 426) and a decoder (950) (column 8 lines 45-50, column 9 lines 21-52, column 15 line 4-41).

Leitch does not explicitly teach 8B/10B. Leitch teaches (Q +S) bits of data wherein Q equals 4 and S equals 2. It would have been obvious to one skilled in the art at the time the invention was made to realize Leitch's Q could equal to 8 and S could equal to 2. One having ordinary skill in the art would be motivated to do so because (a) Leitch teaches that <u>other values</u> of Q and S may be used (column 9 lines 45-47) and (b) such Leitch's other values are not excluded from the inclusion of the value 8 for Q and therefore (Q+S) = (8+2) = 10.

<u>Claims 16-17:</u>

Leitch teaches (figure 18) that the (Q + S) symbols in each of the (R + T) rows are checked for row parity errors (step 1820), the (R + T) symbols in each of the (Q + S) columns are checked for column parity errors (1830). The symbol corrector (940) determines all possible error patterns which satisfy the row and column parity checking results and identifies which of the possible errors are non-ambiguous or ambiguous and corrects such errors therefrom (steps 1840-1870) (column 18 line 59-column 19 line 26, column 15 lines 3-41).

<u>Claims 18-19:</u>

Leitch does not explicitly teach a pre-selected number of iterations of the error-correction routine to the data block is 2. Leitch, however teaches (figure 12) that for each tier, error correction routine is performed (steps 1810 to 1890). It would have been obvious to one skilled in the art would repeatedly process twice (2) for Leitch's

error correction routine. One having ordinary skill in the art would be motivated to do so because such repeatedly process Leitch's error correction routine would depend on the necessity of time and the accuracy of the data error correction.

Claims 20-23:

Claims (20-21) & (22-23) are rejected for reasons similar to those set forth against claims (14-15) & (16-17), respectively.

Response to Arguments

3. Applicant's arguments with respect to claims 1 and 12 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Leitch does not teach (in claim 1) the parity check for each of said N rows and said X column is used for detecting bit level errors. Examiner, however, respectfully traverses applicant's remark.

As state in the art rejection in paragraph 2 above, Cantarella teaches that syndrome bits (S_1, S_2, ...S_{k-1}) from the parity check subcircuits (10, 12, 14) , are decoded in a decoder (20) to produce an output a CVECTOR (C_0, C_1 ... C_{m-1}) which identifies the bit in error in information bits (i_0, i_1, ..., i_{m-1}). Cantarella also teaches that if there is an error, a unique subset of OVP (S_1, S_2, ... S_{k-1}) will be one to identify the bit in error (figure 1, column 4 lines 12-18, column 7 lines 19-59). It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Leitch's row and column parity check results from the row and the column

parity checkers (910 & 930) can later be used for detecting any bit in error (as taught by Cantarella). One having ordinary skill in the art would be motivated to realize so because bit(s) in error(s) have to be detected in order to Cantarella's symbol corrector (940) to correct those error(s) (as taught by Cantarella [column 15 lines 51-60]).

Applicant also argues that Leitch does not teach or suggests identifying at least one a bad byte using a byte-level error detection process. However, such identifying is actually taught by Leitch. Leitch teaches (figure 18) that within each tier (steps 1810, 1880, 1890), the (Q + S) symbols in each of the (R + T) rows are checked for parity errors (step 1820), the (R + T) symbols in each of the (Q + S) columns is checked for parity errors (1830). The symbol corrector (940) determines all possible error patterns which satisfy the row and column parity checking results and identifies which of the possible errors are non-ambiguous or ambiguous and corrects such errors therefrom (steps 1840-1870) (column 18 line 59-column 19 line 26).

For claim 12, applicant also argues that identifying steps identifies the at least one suspect bit using information derived from a byte-level error detection process and information derived from a bit-level error detection process. However, examiner disagrees applicant's position.

Cantarella teaches that syndrome bits (S_1, S_2, ...S_{k-1}) from the parity check subcircuits (10, 12, 14) , are decoded in a decoder (20) to produce an output a CVECTOR (C_0, C_1 ... C_{m-1}) which identifies the bit in error in information bits (i_0, i_1, ...,

i_{m-1}). Cantarella also teaches that if there is an error, a unique subset of OVP (S_1, S_2, ... S_{k-1}) will be one to identify the bit in error (figure 1, column 4 lines 12-18, column 7 lines 19-59).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Leitch's row and column parity check results from the row and the column parity checkers (910 & 930) can later be used for detecting any bit in error (as taught by Cantarella). One having ordinary skill in the art would be motivated to realize so because bit(s) in error(s) have to be detected in order to Cantarella's symbol corrector (940) to correct those error(s) (as taught by Cantarella [column 15 lines 51-60]).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2138

April 1, 2006